Implementation of integrated circuit and design of SAR ADC for fully implantable hearing aids

Jong Hoon Kim\textsuperscript{a}, Jyung Hyun Lee\textsuperscript{b} and Jin-Ho Cho\textsuperscript{c,∗}
\textsuperscript{a}Department of Medical & Biological Engineering, Graduate School, Kyungpook National University, Daegu, Korea
\textsuperscript{b}Department of Biomedical Engineering, School of Medicine, Kyungpook National University, Daegu, Korea
\textsuperscript{c}School of Electronics Engineering, College of IT Engineering, Kyungpook National University, Daegu, Korea

Abstract.

BACKGROUND: The hearing impaired population has been increasing; many people suffer from hearing problems. To deal with this difficulty, various types of hearing aids are being rapidly developed. In particular, fully implantable hearing aids are being actively studied to improve the performance of existing hearing aids and to reduce the stigma of hearing loss patients. It has to be of small size and low-power consumption for easy implantation and long-term use.

OBJECTIVE: The objective of the study was to implement a small size and low-power consumption successive approximation register analog-to-digital converter (SAR ADC) for fully implantable hearing aids.

METHODS: The ADC was selected as the SAR ADC because its analog circuit components are less required by the feedback circuit of the SAR ADC than the sigma-delta ADC which is conventionally used in hearing aids, and it has advantages in the area and power consumption. So, the circuit of SAR ADC is designed considering the speech region of humans because the objective is to deliver the speech signals of humans to hearing loss patients. If the switch of sample and hold works in the on/off positions, the charge injection and clock feedthrough are produced by a parasitic capacitor. These problems affect the linearity of the hold voltage, and as a result, an error of the bit conversion is generated. In order to solve the problem, a CMOS switch that consists of NMOS and PMOS was used, and it reduces the charge injection because the charge carriers in the NMOS and PMOS have inversed polarity. So, 16 bit conversion is performed before the occurrence of the Least Significant Bit (LSB) error. In order to minimize the offset voltage and power consumption of the designed comparator, we designed a preamplifier with current mirror. Therefore, the power consumption was reduced by the power control switch used in the comparator.

RESULTS: The layout of the designed SAR ADC was performed by Virtuoso Layout Editor (Cadence, USA). In the layout result, the size of the designed SAR ADC occupied 124.9 µm × 152.1 µm. The circuit verification was performed by layout versus schematic (LVS) and design rule check (DRC) which are provided by Calibre (Mentor Graphics, USA), and it was confirmed that there was no error. The designed SAR ADC was implemented in SMIC 180 nm CMOS technology. The operation of the manufactured SAR ADC was confirmed by using an oscilloscope. The SAR ADC output was measured using a distortion meter (HM 8027), when applying pure tone sounds of 94 dB SPL at 500, 800, and 1600 Hz regions. As a result, the THD performance of the proposed chip was satisfied with the ANSI s3. 22. 2003 standard.

CONCLUSIONS: We proposed a low-power 16-bit 32 kHz SAR ADC for fully implantable hearing aids. The manufactured SAR ADC based on this design was confirmed to have advantages in power consumption and size through the comparison with

∗Corresponding author: Jin-Ho Cho, School of Electronics Engineering, College of IT Engineering, Kyungpook National University, 680, Gukchaebosang-ro 41944, Daegu, Korea. Tel.: +82 534275538; Fax: +82 534275539; E-mail: jhcho@ee.knu.ac.kr.

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In this paper, we designed a small sized and low-power-consumption SAR ADC for fully implantable hearing aids. The designed SAR ADC consists of sample and hold, a voltage follower, comparator, R-2R ladder digital-to-analog converter (DAC), and SAR logic. The small size and low power consumption are achieved by a DAC based on an R-2R resistor array and comparator using power control switches and offset rejection techniques. The simulation results show that a reference voltage was approximated to the sampled value of the input signal. The SAR ADC is implemented in SMIC 180 nm CMOS technology. The total power consumption is 50 $\mu$W under 1.8 V supply voltage and the core of the SAR ADC occupies 124.9*152.1 $\mu$m.
Table 1
Speech intelligibility for each frequency band

<table>
<thead>
<tr>
<th>Speech frequency [Hz]</th>
<th>Speech intelligibility [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100–500</td>
<td>5</td>
</tr>
<tr>
<td>500–1,000</td>
<td>35</td>
</tr>
<tr>
<td>1,000–2,000</td>
<td>35</td>
</tr>
<tr>
<td>2,000–4,000</td>
<td>13</td>
</tr>
<tr>
<td>4,000–8,000</td>
<td>2</td>
</tr>
</tbody>
</table>

Fig. 1. Graph of audible range.

to 25 dB to meet the input voltage range of the designed ADC. Because the 25 dB amplified 50 mV ac peak signal became an 889 mV ac peak signal, to avoid half wave clipping, the ADC needed an input bias voltage of 900 mV, which is the closest voltage to 889 mV. For the 1.8 v driven ADC, the LSB resolution of the 16 bit ADC is 27.46 µV, and the minimum sound pressure level of the speech area in Fig. 1 is about 45 dB SPL, whose voltage level is equivalent to 622 µV. Therefore, the 16 bit ADC can provide a sufficient resolution to be discriminated even in the 40 dB region. The resolution of the ADC was selected as 16 bit.

The speech and audio application fields generally require a high resolution and slow conversion speed. Therefore, the design target of ADC for fully implantable hearing aids was determined to be 16 bit and 32 kHz. The structure of a typical ADC in accordance with the resolution and conversion speed is shown in Fig. 3, and the ADC structure of advantages and disadvantages according to Fig. 3 is shown in Table 2 [9]. As shown in Fig. 3 and Table 2, the SAR ADC and $\Delta - \Sigma$ ADC conform to the design target. Because of the characteristic of fully implantable hearing aids of being permanently implanted in the body, the ADC of fully implantable hearing aids was selected as an SAR ADC with advantages of power consumption and size.

2.2. Design of SAR ADC

The designed SAR ADC consists of sample and hold, a voltage follower, comparator, and R-2R ladder DAC, as shown in Fig. 4. Therefore, the SAR ADC design focused on low power consumption and a small size.
Fig. 2. Operating characteristics of implantable microphone.

Fig. 3. Minimum sound pressure level of each bit to distinguish speech regions.
Table 2
Advantages & disadvantages of ADC architecture

<table>
<thead>
<tr>
<th>Structure</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
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<tbody>
<tr>
<td>Flash</td>
<td>High speed &amp; latency</td>
<td>Size &amp; resolution &amp; power</td>
</tr>
<tr>
<td>Pipeline</td>
<td>Speed</td>
<td>Latency</td>
</tr>
<tr>
<td>SAR</td>
<td>Power &amp; size</td>
<td>Speed</td>
</tr>
<tr>
<td>Delta-sigma</td>
<td>Resolution</td>
<td>Latency &amp; speed</td>
</tr>
</tbody>
</table>

Fig. 4. Entire circuit diagram of (a) sample and hold, (b) comparator, (c) R-2R ladder DAC, (d) designed SAR ADC.

The designed sample and hold circuit consists of switches, a sampling capacitor, inverter, and voltage follower. If the switch works in the on/off positions, the charge injection and clock feedthrough will be produced by a parasitic capacitor. This problem affects the linearity due to the leakage current. In order to solve the problem of non-linearity, there are ways to reduce the size of the switch and increase the value of the sampling capacitor. However, increasing the value of the sampling capacitor also increases the size and power consumption. In order to reduce the leakage current, the switch size is minimized. In addition, the charge injection is an element that disturbs linearity. In order to prevent the charge injection, a CMOS switch and dummy switch have been used. Because the electric charges of the NMOS and PMOS have opposite polarity, the charge injection is reduced. The non-linearity problem is compensated for by the preceding method, but not completely resolved. Therefore, bit conversion is performed before the occurrence of LSB error due to the non-linearity problem, as shown in Fig. 5. The LSB error is caused in about 7 \( \mu \text{s} \) after the sampling of 2 \( \mu \text{s} \). The clock signal was controlled by 400 ns per 1 bit, and the 16 bit conversion is completed during with 6.4 \( \mu \text{s} \). Thus, a stable output was obtained by the voltage follower of the output stage.

In the SAR ADC, the comparator is a circuit that plays an important role in the ADC as a quantizer of 1 bit, and it produces a digital signal that compared with the output of the sample and hold and the DAC. The structure of the comparator consists of an amplifier, latch and buffer. In order to minimize
the offset voltage and power consumption of the designed comparator, we designed a preamplifier with current mirror. Therefore, the power consumption was reduced by the power control switch used in the comparator. A stable output was obtained by the buffer.

2.3. Simulation of designed SAR ADC

In this paper, we designed an SAR ADC for fully implantable hearing aids. The circuit simulation was performed using the Spectre circuit simulator (Cadence, USA). The simulation result of the designed
Fig. 7. The calculated average power consumption and current simulation of designed SAR DAC.

Fig. 8. Overall layout of designed SAR ADC.

SAR ADC is shown in Fig. 6. As a simulation result, the analog input signal was sampled and was held by a control signal. Thus, the R-2R DAC output has been approximated to the held signal input and we confirmed that the corresponding digital code was output. The current simulation was performed using a circuit simulator Spectre (Cadence, USA), as shown in Fig. 7. The average power consumption was calculated by Eq. (1), which was provided in the simulation software, where $P_{avg}$ is the average power, $P(t)$ is the instantaneous power, and $T$ is the time period. As a simulation result, the power consumption
Table 3

<table>
<thead>
<tr>
<th>Performance table of manufactured SAR ADC</th>
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<tbody>
<tr>
<td>THD</td>
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<tr>
<td>------</td>
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<tr>
<td>1.5%</td>
</tr>
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</table>

Fig. 9. Operation waveform of the designed chip.

3. Results

The layout of the designed SAR ADC was performed by Virtuoso Layout Editor (Cadence, USA), as shown in Fig. 8. In the layout result, the size of the designed SAR ADC occupied 124.9 µm × 152.1 µm. The circuit verification was performed by LVS (layout versus schematic) and DRC (design rule check), and it was confirmed that there was no error. The designed SAR ADC was implemented in SMIC 180 nm CMOS technology. The operation of the manufactured SAR ADC was confirmed by using an oscilloscope, as shown in Fig. 9.

The total harmonic distortion (THD) of the fabricated chip was evaluated by the ANSI s3. 22. 2003 standard. The experimental block-diagram for the THD evaluation is shown in Fig. 10. The SAR ADC output was measured using a distortion meter (HM 8027), when applying pure tone sounds of 94 dB SPL at 500, 800, and 1600 Hz regions. The results of the THD evaluation are shown in Table 3. As a result, the THD performance of the proposed chip was satisfied with the ANSI s3. 22. 2003 standard.

In this paper, the operation of the manufactured SAR ADC for fully implantable hearing aids was verified by using a MSO 4034 oscilloscope (Tektronix, USA) and computer simulation. The performance of the manufactured SAR ADC is shown in Table 4 [10,11]. As a result, the manufactured SAR ADC had an advantage in power and area compared with the conventional ADC and was confirmed to meet the fully implantable hearing aid characteristics.
4. Conclusion

In this paper, we proposed a low-power 16-bit 32 kHz SAR ADC for fully implantable hearing aids. The power consumption is 50 \( \mu \text{W} \) under 1.8 V supply voltage and the core of the SAR ADC occupies 124.9 \( \mu \text{m} \times 152.1 \mu \text{m} \). The manufactured SAR ADC based on this design was confirmed to have advantages in power consumption and size through the comparison with the conventional ADC. Therefore, the manufactured SAR ADC is expected to be used in the implantable medical device field and speech signal processing field, which require small size and low power consumption.

Acknowledgments

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Conflict of interest

None to report.
References


