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Guest-editorial

Special issue: Design and Optimization for High Performance Embedded Systems

Embedded systems and their applications are growing to prevail in our everyday life from commercial electronics, mobile phones, portable health monitoring systems, automobile controllers, robots, smart security devices, to innovative applications that will help the human society in general. The increasingly complicated embedded systems require extensive design automation and optimization tools and techniques. To address this, this special issue includes the extended versions of the five best papers selected from the 2006 IFIP International Conference on Embedded and Ubiquitous Computing (EUC'2006), held in Seoul, Korea, and one invited paper.

The six selected papers cover a variety of subjects in design and optimization for high-performance embedded systems and represent the state-of-the-art techniques in the field:

– In the firs paper titled with "A framework for managing the life-cycle of event-driven, embedded applications", a framework called RISE (Rapid Integrated Solution Enablement) is proposed to ease the complexity of managing the life cycle of event-driven, embedded applications. Event-driven, embedded applications that embody the composition of many disparate components are emerging as an important class of pervasive applications. For solution creation, component composition and software reuse are two central concepts of RISE. Solutions in RISE are graphically composed from reusable components using a visual editor. For deployment and management of solutions, the concept of dynamic and remote deployment of components from the Open Service Gateway Initiative (OSGi) is exploited. The RISE architecture and its prototype implementation, which follows the model-driven methodology and leverages open source technologies, such as Eclipse, are discussed.
– The second paper is titled with "FPGA-Based ROM-Free Network Intrusion Detection Using Shift-OR Circuit". In the paper, the authors introduce a novel FPGA-based signature match co-processor that can serve as the core of a hardware-based network intrusion detection system (NIDS). The co-processor is based on simple shift registers and bitmap encoders for the efficient signature match in hardware. As compared with related work, experimental results show that the proposed work achieves higher throughput and less hardware resource in the FPGA implementations of NIDS systems.
– In the third paper titled with "Energy Minimization for Heterogeneous Wireless Sensor Network", a technique is proposed to minimize the total energy consumption for sensor network with a probabilistic random variable model. Due to the uncertainties in execution time of some tasks, the paper models each varied execution time as a probabilistic random variable with the consideration of applications' performance requirements to solve the MAP (Mode Assignment with Probability) problem. Using probabilistic design, an optimal algorithm is proposed to minimize the total energy consumption while satisfying the timing constraint with a guaranteed confidence probability. The experimental results show that the approach achieves significant energy saving than previous work.
– In the fourth paper titled with "Hardware-Software Co-design of a Speech Translation Embedded System", the authors propose a hardware-software co-design of a speech translation embedded system for portable S2ST (speech-to-speech translation)

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applications. The system is characterized by small size, low cost, real-time operation, and high portability. In order to realize the proposed S2ST system, an ARM-based system-on-a-programmable-chip (SoPC) architecture, the speech translation intellectual property and the software procedures of the proposed SoPC are designed. The entire design was implemented on ALTERA EPXA10. The English-to-Mandarin translation process can be completed within 0.5 second at a 40 MHz clock frequency with 1,200 translation patterns. The maximum frequency is 46.22 MHz, and the usage of logic elements is 19,318 (50% of the total number of logic elements of the EPXA10 device).

– In the fifth paper titled with "A Low-Power Baseband Modem Architecture for a Mobile RFID Reader", the authors present an architecture overview of a multi-protocol RFID reader on mobile devices with detailed description of hardware implementation. In the design, several design parameters, such as low power consumption, cost effectiveness and flexibility are considered. The architecture supports WIPI (Wireless Internet Platform for Interoperability); therefore, any WIPI application can use our RFID reader's functionalities to query tags' information from Internet through HAL interfaces. The system is implemented on the ARM-based Excalibur FPGA with iPAQ PDA, and also a chip with 0.18um technology for verification of the architecture.
– In the sixth paper titled with "Asymmetry-Aware Link Layer Services in Wireless Sensor Networks", the authors propose two asymmetry-aware link layer services, including the neighborhood link quality service (NLQS) and the link relay service (LRS) for sensor network. The novelty of the NLQS service is taking the link asymmetry into consideration, providing timeliness link quality and distinguishing the inbound and outbound neighbors with the support of LRS, which builds a relay framework to alleviate the effects of link asymmetry. To demonstrate the proposed link layer service, two example applications, building the shortest-hop routing path (SHRT) and the best path reliability routing path (BRRT), are implemented on the TinyOS platform. The experimental results show that the performance of two example applications is improved substantially.

Finally, we would like to take this opportunity to thank the authors for their contributions to this special issue, and the EUC'06 program committee for their excellent work in organizing the conference. In particular, we would like to thank EUC'06 steering chairs, Prof. Laurence T. Yang and Prof. Minyi Guo, for their help in preparing this special issue.

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