

Analog front-end measuring biopotential signal with effective offset rejection loop

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Abstract. This paper presents an analog front-end (AFE) IC design for recording biopotential signals. The AFE employs a capacitively coupled instrumentation amplifier to achieve a low-noise and high-common mode rejection ratio (CMRR) system. A ripple reduction loop is proposed to reduce the ripple generated by the up-modulating chopper. The low frequency noise is attenuated by an input AC coupling capacitor, and is attenuated again by a DC servo loop. The proposed AFE features a differential gain of 71 dB, and a CMRR of 89 dB, at 50 Hz. Furthermore, the proposed AFE can robustly acquire biopotential signals even in the presence of an input offset and ripples.

Keywords: Biopotential analog front-end (AFE), electroencephalograph (EEG), electrocardiogram (ECG), ripple reduction loop, DC servo loop

1. Introduction

There has been a growing interest in biopotential acquisition systems for improving the quality of daily life [1]. Because biopotential acquisition devices used in hospitals are bulky and weighty, miniaturized and portable biopotential monitoring systems are required to record signals while causing minimal discomfort. The biopotential signals such as electroencephalogram (EEG) and electrocardiogram (ECG) have small signal amplitudes less than a few mV in low frequency, thus a low-noise and high CMRR amplifier is required to record high-quality biopotential signals [2]. A capacitively coupled chopper instrumentation amplifier (CCIA) provides efficient topology for these specifications [3]. However, the chopper stabilization employed in the CCIA generates ripple at the instrumentation amplifier (IA) output, due to the up-modulated input offset of the IA [4]. Additionally, the mismatch between the electrodes and the polarization of the Ag/AgCl electrodes generates an external offset voltage, which can cause the oversaturation of the IA output.

This paper presents an analog front-end (AFE) IC for recording biopotential signals. The AFE employs the CCIA with multiple feedback loops, which compensate for analog imperfections such as the external offset in the input electrodes and the internal offset in the CCIA; the two feedback loops, a ripple rejection loop (RRL) and a DC servo loop (DSL) are designed to cancel these offsets. In the proposed CCIA, the offset due to the electrode mismatch is inherently attenuated by the AC-coupled

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input stage without DSL. However, DSL is still effective for the reduction of the low-frequency noise and low-frequency signal artifact such as a respiration signal. Thus, an additional DSL is also designed to provide additional poles for the overall transfer function of the CCIA, and form an additional high-pass filter (HPF). As a result, the input offset and low-frequency artifacts are attenuated by a second-order HPF (CCIA + DSL), in contrast to the first order attenuation used in previous studies [5].

2. Proposed analog front-end

The proposed analog front-end (AFE) is shown in Figure 1. The AFE includes the IAs of two stages and fourth order low pass filter (LPF) using a Sallen-Key topology. Each stage of the IA is formed by the CCIA, RRL, and DSL, providing a gain ranging from 23.56 dB to 35.69 dB. The LPF suppresses the high frequency noise associated with chopping. The cutoff frequency of the LPF is controlled from 100 Hz to 200 Hz.

Figure 2 shows a simplified schematic of the proposed CCIA. The AC-coupling capacitor blocks the DC offset from the electrodes. The feedback capacitor, C_f , is programmable to adjust the gain of the CCIA. As in Figure 1, the feedback resistor, R_f , should be very large at the appropriate input bias point to achieve linear amplification. In this work, R_f is implemented by a pseudo-resistor using a well-known MOS-bipolar device to achieve an impedance greater than 100 G Ω . The large impedance of the pseudo-resistor can reduce the output non-linearity due to the non-linear resistance of the pseudo-resistor, as shown in Figure 1. The fully differential amplifier employed in the CCIA is a rail-to-rail, constant g_m , folded cascode amplifier with a class-A output stage to provide a wide output swing.

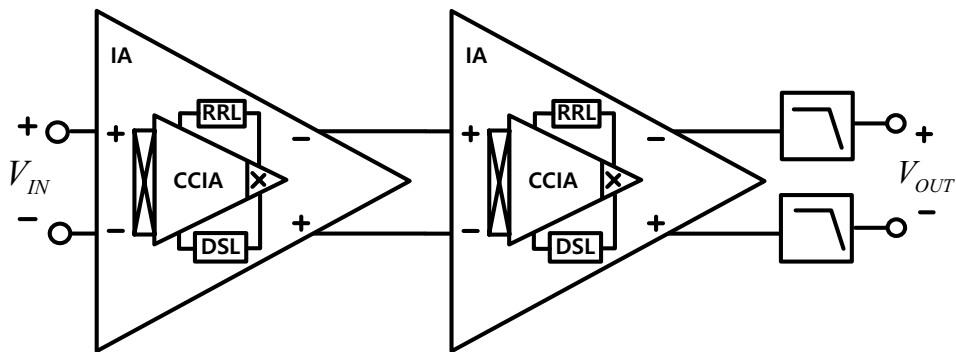


Fig. 1. Proposed analog front-end.

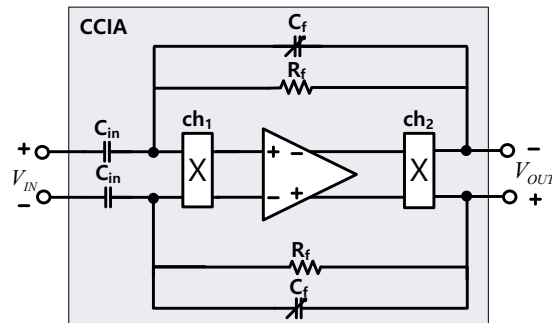


Fig. 2. Schematic of the proposed CCIA.

$$\frac{v_{OUT}}{v_{IN}} = \frac{sC_{in}R_f}{1 + sC_fR_f} = \frac{sC_{in}}{\frac{1}{R_f} + sC_f} \quad (1)$$

Figure 3 shows the fourth order low pass filter (LPF) using a Sallen-Key topology. The LPF removes glitches and the high-frequency noise from the biopotential signal amplified by the IAs. The transfer function of LPF is expressed as:

$$\frac{v_{OUT}}{v_{IN}} = \left(\frac{1}{1 + sC_1(R_1 + R_2) + s^2C_1C_2R_1R_2} \right)^2 \quad (2)$$

Therefore, the overall transfer function of the AFE is expressed as:

$$\frac{v_{OUT}}{v_{IN}} = \left(\frac{sC_{in}R_f}{1 + sC_fR_f} \right)^2 \left(\frac{1}{1 + sC_1(R_1 + R_2) + s^2C_1C_2R_1R_2} \right)^2 \quad (3)$$

2.1. Ripple reduction loop

Figure 4 shows a simplified block diagram of the CCIA with the RRL. When an offset voltage, V_{OS} , is present as shown in Figure 4, a ripple is generated at V_{OUT} by the up-modulating chopper, ch_2 . This ripple is demodulated to a low frequency by the feedback chopper, ch_3 , and is filtered by a Miller integrator. C_{OL1} converts the filtered voltage into a current that is fed back to the input of the CCIA. The feedback current is modulated by the chopper, ch_4 , and is demodulated by the chopper, ch_1 . Thus, the offset in front of the amplifier, V_{OS} , is rejected by this negative feedback loop. Consequently, the ripple caused by the offset voltage is reduced. Here, the RRL does not affect the transfer function for the low-frequency range because the RRL operates as a notch filter at the chopper frequency, from the perspective of the demodulated output signal.

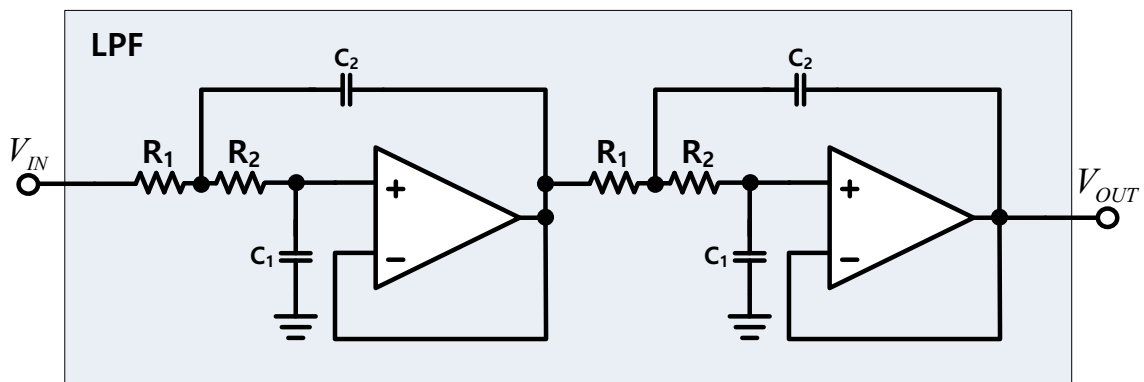


Fig. 3. Fourth order LPF of Sallen-Key topology.

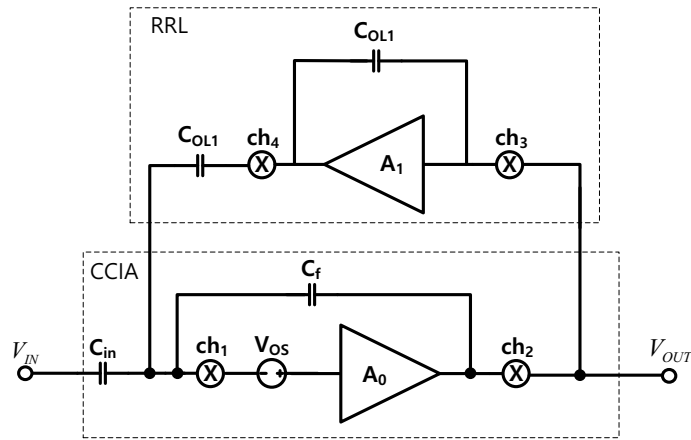


Fig. 4. Simplified block diagram of the RRL and CCIA.

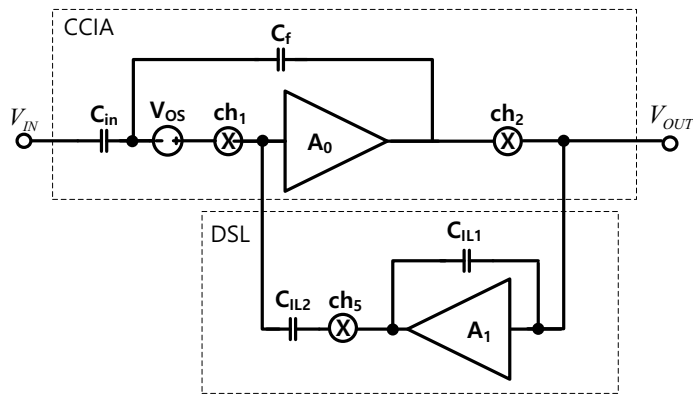


Fig. 5. Simplified block diagram of the CCIA and DSL.

2.2. DC servo loop

In the proposed CCIA, the input DC offset is inherently attenuated by the AC-coupling capacitor C_{in} . However, respiration artifact and other low-frequency noise cannot be rejected completely with the sole HPF characteristics of the CCIA; thus, an additional DSL is designed. Figure 5 shows a simplified block diagram of the CCIA with the DSL. Assuming an offset voltage and low-frequency artifacts, V_{OS} is attenuated by the first-order HPF, as shown in Figure 5. However, the remaining low-frequency signal is modulated by ch_1 , demodulated by ch_2 , and filtered by the Miller integrator. The output of the Miller integrator is modulated to a high frequency by ch_5 and converted into a current that is fed back to the CCIA by C_{IL2} . During this negative feedback process, V_{OS} is rejected. Here, the DSL operates as an additional HPF in the input stage.

3. Results and discussions

Figure 6 illustrates the layout of the proposed circuit, which includes the biopotential AFE and 12-bit successive approximation register (SAR) analog-to-digital converter (ADC). When the offset volt-

age causes a ripple, the output can be saturated. The proposed RRL reduces the ripple to obtain a suitable output signal. Figure 7 shows the effect of the RRL when an offset voltage of 10mV is present. Over time the ripple decreases, and a sinusoidal wave (without ripple) is observed after 1 second at a steady state. Figure 8 illustrates the effect of the DSL. When the DSL operates, it adds additional poles to the input HPF; thus, the cutoff frequency of the IA adjusts to 3.2 Hz, rejecting the low-frequency noise and respiration artifact. Figure 9 illustrates the differential gain and CMRR of the IA. The Ag/AgCl electrode is modeled utilizing a 51 k Ω resistor and 47 nF capacitor connected in parallel. A CMRR simulation is performed under the worst-case input mismatch condition. The electrode impedance model is connected to only one input IA port. Assuming the modeled electrode is connected to only one of the two IA inputs, the mismatch demonstrates the worst-case scenario. In this situation, a differential gain of 71 dB and a CMRR of 89 dB are observed at 50 Hz.

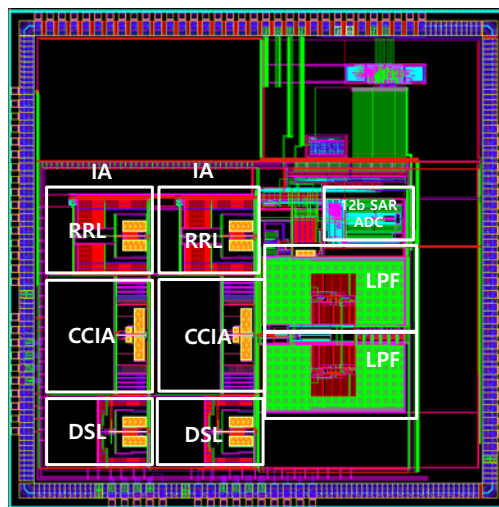
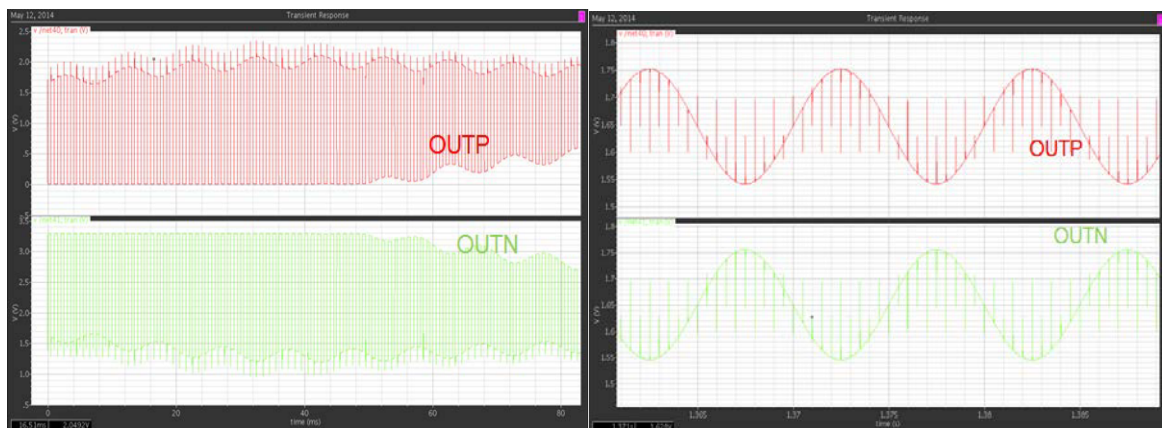


Fig. 6. Layout view.



(a) Initial transient response: 0-80 ms.

(b) Steady-state response (after 1 s).

Fig. 7. Effect of the RRL.

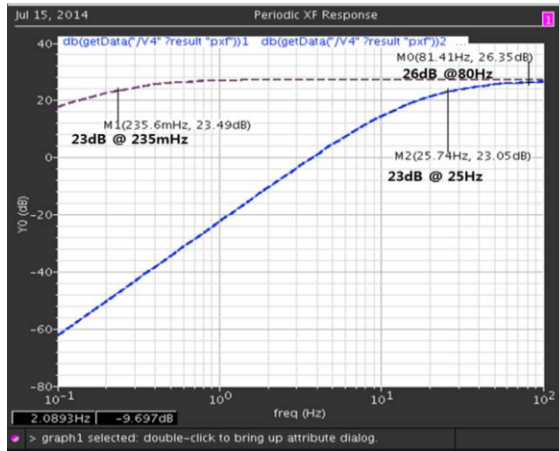


Fig. 8. Effect of the DSL.

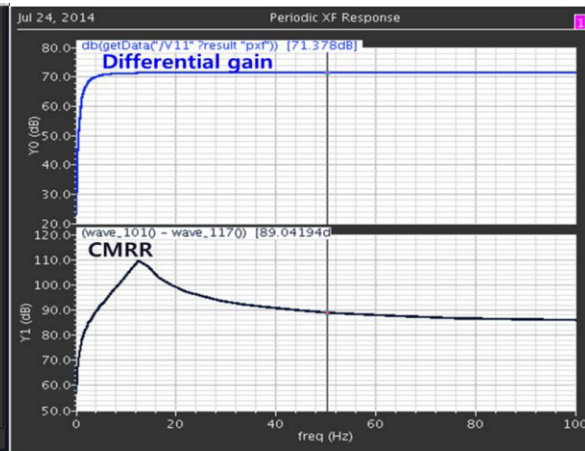


Fig. 9. Differential gain and CMRR of the two stage IAs.

Table 1
Performance Summary

	[4]	[5]	This work
Technology	0.7 μm	65nm	0.18 μm
Supply current (μA)	230	1.8	30
Supply voltage (V)	5	1	3.3
AC offset reduction	First-order reduction with the Miller integrator	First-order reduction with the SC integrator	First-order reduction with the Miller integrator
DC offset cancelation	Not included	First-order reduction	Second-order reduction
CMRR (dB)	120	134	89
Input noise ($\text{nV}/\sqrt{\text{Hz}}$)	Not available	60	160

4. Conclusion

A biopotential acquisition AFE IC is presented. To reject the offset voltage, low-frequency noise, and respiration artifact, the ripple reduction loop (RRL) and DC servo loop (DSL) are proposed. The results demonstrate that the RRL and DSL effectively reject the ripples and low-frequency noise, respectively. The performance comparisons are given in Table 1 [4, 5]. The differential gain and CMRR of the proposed IA are 71 dB and 89 dB, respectively, at 50 Hz.

Acknowledgments

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