

Erratum

Special Issue: PATMOS 2007 selected papers on low power electronics

Nadine Azemard* and Lars Svensson
[Journal of Embedded Computing 3(3) (2009)]

When this special issue was originally published, the guest-editorial was omitted. It is now reproduced here.

Guest-editorial

PATMOS'07, the seventeenth in a series of international workshops, took place at Gothenburg, Sweden, September 3-5, 2007. Over the years, the PATMOS meeting has evolved into an important European event, where industry and academia meet to discuss power and timing aspects in modern integrated circuits and system design. The PATMOS objective is to provide a forum to discuss and investigate the emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems. The technical program focuses on timing, performance, and power consumption as well as architectural aspects with particular emphasis on modelling, design, characterisation, analysis and optimization.

A selection of the papers on low power electronics presented at the PATMOS 2007 is included in this special issue of the Journal of Embedded Computing (JEC). The JEC addresses the most innovative developments in the area of embedding computing include

all aspects of embedded computing systems with emphasis on algorithms, systems, models, compilers, architectures, tools, design methodologies, test and applications. The selection of the papers has been done based on the peer reviews of the PATMOS workshop, the quality of the presentations and the feedback and comments received during and following the workshop.

The papers included in this special issue are extended and updated versions of the original PATMOS papers. This special issue combines a workshop focused on power and power optimization with a journal targeting the same technologies. The intention is the dissemination of the latest research results in the area of embedding computing on low power and power optimizations.

Nadine Azemard

Patmos'07, Program Chair
LIRMM, UMR CNRS/University of Montpellier
Nadine.Azemard@lirmm.fr

Lars Svensson
Patmos'07, General Chair
Chalmers University of Technology
larssv@ce.chalmers.se

*Corresponding author. E-mail: Nadine.Azemard@lirmm.fr.



Nadine Azemard received the M.S. degree and the Ph.D. degree in Electronics from the University of Science of Montpellier, France, in 1987 and 1990, respectively. In 1991 she joined the CNRS and the Laboratory of Computer Sciences, Robotics and Microelectronics of Montpellier as a searcher. Her current field of research includes timing and power modeling and estimation, statistical timing analysis, performance optimization of CMOS circuits under constraints, low power design. She is also in charged of the development of timing analysis and optimization engine.



Lars Svensson Lars Svensson is an Associate Professor at Chalmers University, Sweden. He received his Ph.D degree from Lund University, Sweden, in 1990; since then, he has worked both in industry and in academia in Europe as well as in the United States. His research interests are low-power circuit design and low-level processor architecture.