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Guest-editorial

Adaptive hardware/evolvable hardware – The state of the art and the prospectus for future development

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With great pleasure, we would like to welcome you to this special issue of the *International Journal of Knowledge-based and Intelligent Engineering Systems*. The motivation of its selected topic – Adaptive Hardware/Evolvable Hardware – the State of the Art and the Prospectus for Future Development – is deeply justified. Nevertheless, it is hardware implementation of the most benefit for the society and indeed most revolutionizing application of E*volutionary* C*omputation* (EC) by leading to the so-called *Evolvable Hardware* (EHW). These new EC based methodologies make possible the hardware implementation of both genetic encoding and artificial evolution, having a new brand of machines as a result.

This type of machine is evolved to attain a desired behaviour that means they have a *behavioural computational intelligence*. There is no more difference between adaptation and design concerning these machines, these two concepts representing no longer opposite concepts. A dream of technology far years ago currently became reality: adaptation transfer from software to hardware is possible by the end. Much more, the electronics engineering as a profession was radically changed: the most based on soldering assembling manufacturing technologies are largely replaced now by programming circuitry-based technologies, including EHW technologies.

This new design methodology for the electronic circuits and systems is not a fashion. It is suitable to the special uncertain, imprecise or incomplete defined real-world problems, claiming a continuous adaptation and evolution too. An increased efficiency of the methodology may be obtained by its application in the soft computing framework that means in aggregation with other intelligent technologies such as fuzzy logic (FS) and neural networks (NN), Artificial Immune Systems (AIS), evolutionary algorithms (EA).

Dramatic changes happen in the relation between hardware and the application environment, and this in case of *malicious faults* or need for *emergent new functions* that claim for in-situ synthesis of a totally new hardware configuration. EHW is suitable for flexibility and survivability of autonomous systems. EHW *survivability* means to maintain functionality coping with changes in hardware characteristics under the circumstances of adverse environmental conditions as for example: temperature variations, radiation impacts, aging and malfunctions. EHW *flexibility* means the availability to create new functionality required by changes in requirements or environment.

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The application developer may meet different design tasks to be evolved. As the case, the design to be evolved could be: a program, a model of hardware or the hardware itself. Algorithms that run outside the reconfigurable hardware, mainly feature the actual EHW state of the art, but also some chip level attempts were done.

It is important to understand that *evolutionary circuit design* and *evolvable hardware* (EHW) are two different and distinct approaches. *Evolutionary circuit design* performs the evolution (the design) of a single circuit. The aim is typically to design novel implementations that are better (in terms of area, speed, power consumption) than conventional deigns and/or to design circuits with additional features such as fault-tolerance, testability, polymorphic behaviour, that are difficult to design by conventional methods.

Evolvable hardware(EHW) involves an EC responsible for continual adaptation. EHW is applied to high-performance and adaptive systems in which the problem specification is unknown beforehand and can vary in time.

An EHW system, any is its destination, either for demonstrations, prototype experiments or real time implementation, must be structured in from of two main components: the *reconfigurable hardware* (RH) and the *reconfigurable mechanism* (RM).

In a larger context, EHW is seen as a special case of the A*daptive* H*ardware* (AH), as it is driven mainly by internal objectives and its performance continuouslyimproves over time. The three AH structural components are: hardware that can change (HW), controller that can change the hardware (CO) and the objective function (OF). In the most largest context, AH is seen as a special case of A*daptive* S*ystems* (AS) due to the capacity to modify itself to maintain or improve its performance towards an internal objective and/or in response to a changing operating environment. The two AS structural components are the CO and OF. So the largest context frames the EHW as a special case of AS.

We are indebted to the authors and reviewers for their efforts, outstanding contributions and assistance in the preparation of this special issue. We would like to express our sincere gratitude to The KES Advisory Group and to Dr. Robert J. Howlett - the KES Executive Chair for giving us the opportunity to edit this special issue.

This special edition consists of six papers. In the first paper, Torresen is focussed on a new method that reduces the problem of limited scalability for designing electronic circuits. A novel digital EHW architecture for signal classification has been developed that allows for incremental evolution. It is based on initially evolving sub circuits for each category to be detected, followed by a step where the complete system is further optimized with evolution. The architecture is applied for classifying sensor data in a prosthetic hand controller. Analysis of the best circuit shows the importance of having an architecture containing some gates with random connections as well as allowing for incremental evolution to get the highest possible performance. The best circuit evolved shows a much better performance than what was obtained by artificial neural networks. The results illustrate that this is a promising approach for evolving systems for complex real world applications.

The second paper by Upegui et al. introduces a project funded by the EU omission and regroups eight research institutes from four countries. The Perplexus hardware platform is a scalable computing substrate made of custom reconfigurable devices endowed with bioinspired capabilities. The modularity and flexibility of the platform is the key for tackling the diverse hardware setup needs of different applications. The Perplexus platform will provide a novel modelling framework thanks to the pervasive nature of the hardware platform, its bio inspired capabilities, its strong interaction with the environment and its dynamic topology. The final structure will be used as a simulation tool for three applications: neurobiological modelling, culture dissemination modelling and cooperative collective robotics. In this paper the authors have introduced *ubidule* a modular and customizable pervasive device whose core is the *ubichip* – a reconfigurable electronic chip capable of implementing bio-inspired hardware systems featuring growth, learning and evolution. They have presented also the architectural and reconfigurability mechanisms that will allow an efficient implementation of such systems. These mechanisms are dynamic routing, distributed self-reconfiguration, and a neural-friendly logic cell architecture, keeping in mind the scalability issues that rise in the implementation of such type of complex systems.

Stauffer et al. deal with the functional design of self-organizing bio inspired systems involving several mechanisms, whose growth and branching processes are based on the Tom Thumb algorithm. These mechanisms allow the cellular systems to perform cloning (cellular and organismic self-replication), cicatrisation (self-repair), and regeneration (organismic self-repair). The hardware design of self-organizing bio inspired

systems results from the implementation of the processes constituting the precedent mechanisms. This implementation is realized with the help of VHDL description language, as a data and signals cellular automaton (DSCA).

The computational development is one of the approaches in the evolutionary design techniques that tries to overcome the problem of scale. This approach is treated by Bidlo and Skarvada. The problem of scale means how to create a large complex solution and represents a significant obstacle for the evolution of complex extensive systems. The authors present an instruction-based developmental method for the evolutionary design of generic structures of digital circuits. The developmental system involves a set of application-specific instructions constituting programs in order to solve a given task. In particular, the goal is to construct generic structures of combinational circuits. An evolutionary algorithm is utilized for the design of these programs that represents a mapping from the genotypes to the phenotypes during the evolutionary process, in fact the prescription for thieve a routing power saving of e construction of target circuits. Two case-studies are presented in order to demonstrate the successfulness of this approach: the evolutionary design of generic combinational multipliers and the evolutionary design of generic sorting networks.

In the fifth paper, Fung and Arslan are focussed on some aspects of the CAD design process of reconfigurable devices. They present a novel method to gain power savings during the placement stage of CAD flow. The proposed system modelled the number of switches used in the circuit and employed simulation annealing algorithm to reduce the overall routing power. The system was tested against 8 large benchmark circuits. It was able to achieve a routing power saving of up to 18% compared with cases without modelling the switches. This paper has presented not only the switch modelling technique where it examines the routing resource early in the placement stage of designing reconfigurable devices to save routing power. The paper also reviews the sources of power dissipation which include both static and dynamic power.

Hintea, Csikpes et al. in the six paper deal with a novel approach to the design of integrated reconfigurable and analog programmable filters for commercial mobile applications. The operation principles are built around the synthesis method using state variables and the functional emulation of a passive ladder prototype. The method is described in the specific context of an analog filter which is capable of operating in both the real and complex domains; the filter is designed using the OTA-C technique, features a programmable order and transfer function and is envisioned as part of a combined low

IF/ zero IF receiver architecture for a software defined radio transceiver. The novel method is demonstrated by presenting the simulation results of the real low pass/ complex band pass filter for a 0.5 dB Chebyschev approximation. The highly modular filter topology, together with the elaborated switch network, allows the implementation of low pass or complex band pass transfer functions of different orders and various values for the specific frequency parameters. The adjustment of the frequency parameters is done independently on the approximation and the filter order.

We believe these six papers form an interesting snapshot of the state of the art in the AH/EHW area and we hope readers find them useful and rewarding.