

Application of Concurrency to System Design, the Sixth Special Issue

Preface

The seventh International Conference on the Application of Concurrency to System Design (ACSD) was held in July 2007 in Bratislava, Slovakia. It has become a tradition that *Fundamenta Informaticae* publishes a special issue with revised and extended versions of a selection of the best papers from ACSD. The current issue is the sixth special issue devoted to ACSD.

ACSD serves as a forum for disseminating theoretical results with application potential and advanced methods and tools for the design of complex concurrent systems. The conference aims at cross-fertilizing both theoretical and applied research on the following topics:

- design methods, tools and techniques based on models of computation and concurrency (dataflow models, communicating automata, Petri nets, process algebras, state charts, MSCs, etc.), (performance) analysis, verification, testing and synthesis;
- hardware / software co-design, platform-based design, component-based design, refinement techniques, hardware / software abstractions, co-simulation and verification;
- synchronous and asynchronous design, asynchronous circuits, globally asynchronous locally synchronous systems, interface design, multi-clock systems, functional and timing verification;
- concurrency issues in systems-on-chip, massively parallel architectures, networks on chip, task and communication scheduling, resource, memory and power management, fault-tolerance and quality-of-service issues;
- (industrial) case studies of general interest, gaming applications, consumer electronics and multimedia, automotive systems, (bio-)medical applications, internet and grid computing, etc.;
- concurrency issues in ad-hoc, mobile and wireless networking, sensor networks, communication protocols, cross-layer optimization, resource, power and quality-of-service management, fault-tolerance, concurrency-related security issues;
- concurrency in business process management, business process modeling, simulation and verification, (distributed) workflow execution, business process (de-) composition, interorganizational and heterogeneous workflow systems, computer-supported collaborative work systems, web services;

- synthesis and control of concurrent systems, (compositional) modeling and design, (modular) synthesis and analysis, distributed simulation and implementation, (distributed) controller synthesis, adaptive systems, supervisory control.

The six papers in this special issue have been selected from the papers presented at the seventh ACSD conference. ACSD 2007 had 42 regular submissions. Every submission was reviewed by at least three specialists in the subject area of the paper. Seventeen submissions (40%) were selected for presentation at the conference and publication in the IEEE CS Press proceedings. The selection for this special issue was based on the reviews of the ACSD program committee and the presentations at the conference.

The authors of the selected papers were invited to submit extended and revised versions of their work to this special issue. The extended papers have each been reviewed by at least three reviewers. At least two of those reviewers did not review the ACSD version of the paper. Reviewers were asked to pay special attention to novelty and originality, also with respect to the ACSD versions of the papers. Papers were revised according to the suggestions of the reviewers.

This special issue presents the papers according to the alphabetical order of the last names of the first authors.

The first paper, by Frédéric Béal, Tomohiro Yoneda, and Chris J. Myers, proposes a new solution to the hazard checking problem for timed asynchronous circuits. Earlier approaches are too slow, overly pessimistic, or cannot handle circuits with loops. The presented approach is based on a new framework for conservative design representation related to abstract interpretation and a novel semantics for timed asynchronous circuits. The resulting solution to the hazard detection problem is conservative without being too pessimistic and it is efficient. The approach also allows to eliminate part of the detected hazards.

The next paper, by Robin Bergenthum, Jörg Desel, Robert Lorenz, and Sebastian Mauser presents two methods to synthesize Petri nets, in particular, place/transition nets from finite partial languages or sets of labeled partial orders. Partial orders truly represent the concurrency among the events of a system. The work is the first to provide an effective solution to the synthesis problem for place/transition nets when starting from their partial-order behavior. The techniques have a wide application potential, ranging from hardware design to workflow management.

In the third paper, Hanifa Boucheneb and Hind Rakkay propose a new abstraction for time Petri nets that preserves linear-time temporal logic (LTL) formulae. It uses bisimulation equivalence on state classes to provide a compact state-class graph that is smaller and more efficient to compute than earlier abstractions. The authors show that the abstraction can be combined effectively with partial-order reduction techniques, and that it allows model checking of time Petri nets.

Franck Cassez and Stavros Tripakis address fault diagnosis by static and dynamic observers in the fourth paper. The basic problem of diagnosability is the question of whether an observer is capable of identifying a fault given a set of sensed events. The main results of the paper are related to the minimization of the number of sensed events required for diagnosability for a static observer that cannot change the set of observed events during execution, and to the synthesis of dynamic observers that can switch sensors on and off during execution, thus dynamically changing the set of observed events. Solutions to these problems are presented, and several complexity results are proven.

The fifth paper, by Victor Khomenko, Mark Schaefer, and Walter Vogler, presents developments that are useful to improve the efficiency of asynchronous-circuit synthesis. The paper develops a theory for signal-transition graphs (STGs) with dummy transitions and OR-causality. The theory is based on the

notion of output determinacy, which is a relaxation of determinism essentially stating that circuit outputs are always precisely determined. To illustrate the applicability of the theory, the paper presents an STG decomposition algorithm that alleviates the state-space explosion that occurs during circuit synthesis.

Finally, in the sixth paper, Danil Sokolov, Ivan Poliakov, and Alex Yakovlev, develop four different semantics for asynchronous data path circuits. It is argued that the proposed hybrid semantics, that combines aspects of two other semantics, exhibits good expressivity while not resulting in excessive model complexity. A translation to Petri nets is provided, that makes the rich body of Petri-net analysis methods and tools available for analyzing asynchronous data paths. A tool framework is presented, and analysis results show the application potential of the developed results.

We thank the authors of the six papers of this special issue for their efforts to produce interesting and useful contributions. We are grateful to the reviewers, both of the conference versions of the papers and of the extended journal versions published in this issue, for their careful reviews and valuable suggestions. We hope the end result is worthwhile reading.

Special Issue Editors

Twan Basten

Department of Electrical Engineering
Eindhoven University of Technology
Den Dolech 2, 5612 AZ, Eindhoven, The Netherlands
a.a.basten@tue.nl

Ryszard Janicki

Department of Computing and Software
McMaster University
Hamilton, Ontario, Canada L8S 4K1
janicki@cas.mcmaster.ca